REMARKS

No new matter has been added. The Applicants again request entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,

Brick G. Power
Registration No. 38,581
Attorney for Applicants
TRASKBRITT
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: March 14, 2002
BGP/dn
N:\2269\4296.1\PRELIM.AMD

Enclosures: Version of Specification with Markings to Show Changes Made
Version of Claims with Markings to Show Changes Made

VERSION OF SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

Please replace the title of the invention on Page 1 as follows:

[DIE TO DIE]DIE-TO-DIE CONNECTION METHOD AND ASSEMBLIES AND PACKAGES INCLUDING DICE SO CONNECTED

Please replace the title of the invention on page 2 as follows:

[DIE TO DIE]DIE-TO-DIE CONNECTION METHOD AND ASSEMBLIES AND PACKAGES INCLUDING DICE SO CONNECTED

Please replace Paragraph **[0008]** as follows:

[0008] Keeping in mind the trend toward faster computers and other electronic devices, the use of intermediate conductive elements, such as wire bonds, and the conductive traces of carrier substrates to electrically connect the semiconductor dice of a multi-chip module is somewhat undesirable since the electrical paths of these types of connections are typically lengthy and, consequently, limit the speed with which the semiconductor dice of the multi-chip module may communicate with one another. The [effects]affects that these types of connections in conventional multi-chip modules have on the speed at which an electronic device, such as a computer, operates are particularly undesirable when one of the semiconductor dice of the multi-chip module is a microprocessor and the other semiconductor dice of the multi-chip module are semiconductor devices with which the microprocessor should quickly communicate.

Please replace Paragraph **[0009]** as follows:

[0009] The so-called system-on-a-chip (SOC) has been developed to increase the speed with which two semiconductor devices, such as a logic device (e.g., a microprocessor) and a memory device, communicate. Each of the semiconductor devices of a SOC structure are fabricated on the same substrate, providing very short connections with reduced contact resistance between two or more devices. The speed with which the two devices communicate is,

therefore, increased relative to the speeds with which the separate semiconductor devices of conventional assemblies communicate.

Please replace Paragraph **[0041]** as follows:

[0041] As corresponding bond pads 14 and 24 are electrically connected to one another by way of conductive structures 28, the physical lengths of electrical circuits including conductive structures 28 are much shorter than the physical lengths of circuits including wire bonds or conductive traces of carrier substrates, as have been employed in conventional multi-chip modules. Accordingly, first semiconductor die 10 may communicate with connected semiconductor dice, such as second semiconductor die 20, at much faster rates than are possible with conventional multi-chip modules.

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method for interconnecting at least two semiconductor dice, comprising:

providing a first semiconductor die including a plurality of bond pads arranged in an array over an active surface thereof;

providing at least one second semiconductor die including a plurality of bond pads on an active surface thereof;

orienting said first semiconductor die and said at least one second semiconductor die with said active surfaces thereof facing each other;

electrically connecting at least some bond pads of said plurality of bond pads of said at least one second semiconductor die with corresponding bond pads of said plurality of bond pads of said first semiconductor die.

11. The method of claim 10, wherein said providing said carrier substrate comprises providing [a]said carrier substrate with at least one recess formed in said surface.

16. (Amended) The method of claim 14, wherein said disposing said conductive [structures]elements between said other bond pads of said first semiconductor die and said corresponding contacts of said carrier comprises providing a quantity of a material comprising at least one of a metal, an alloy, a conductive epoxy, a conductor-filled epoxy, and a z-axis conductive elastomer.

32. (Amended) The method of claim 23, wherein said providing said carrier comprises providing a plurality of leads, each of said plurality of leads corresponding to said bond pads of said first semiconductor die exposed beyond [an]said outer periphery of said at least one second semiconductor die.

33. (Amended) The method of claim 29, wherein:

said providing said first semiconductor die comprises providing said first semiconductor die with a first member of a conductive element secured to each bond pad thereof that is located beyond [an]said outer periphery of said at least one second semiconductor die; and

said providing said carrier substrate comprises providing said carrier substrate with a second member of said conductive element secured to each corresponding contact pad thereof.

34. (Amended) The method of claim 33, further comprising aligning at least said first and second members of said conductive [structure]element.

35. (Amended) The method of claim 34, further comprising securing at least said first and second members of said conductive [structure]element to each other.